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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,717	09/30/2003	Robert H. Utley	2	6318

7590 12/12/2005

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EXAMINER	
GU, SHAWN X	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,717	UTLEY, ROBERT H.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10 and 13-17* is/are rejected.

7)☒ Claim(s) *7-9,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003 and 24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 30 September 2003 was filed after the mailing date of the application on 30 September 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 1, 16 and 17, it is unclear to the Examiner if the "alternating manner of accessing" reduces the likelihood of access conflicts between the banks when

compared to non-alternating manner of accessing or some other manner of accessing. Further clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 10 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. [US 6,745,277 B1] (hereinafter "Lee"), further in view of Beshai et al. [US 6,907,002 B2] (hereinafter "Beshai").

As for claims 1, 16 and 17, Lee teaches a processor (Fig 1, 100 System Controller; Fig 2) comprising:

controller circuitry operative to control the storage of a plurality of separate groups of protocol data units (Fig 1, Packet #1 to #4 each in a group; Fig 3, Packet #2 and #5 in one group, Packet #1, #3 and #4 each in a group) received by the processor;

the groups of protocol data units being storable in memory circuitry (Fig 1 and Fig 3, 114 Multibank Memory) associated with the processor;

wherein the memory circuitry is arranged in a plurality of banks (Fig 1 and Fig 3, B1-B4 in 114), the plurality of banks being configured to store respective ones of the plurality of separate groups of protocol data units, such that each of the plurality of the banks stores a corresponding one of the plurality of the separate groups of protocol data units (Fig 1 and Fig 3, 114 Multibank Memory); and

wherein the groups of protocol data units are accessed in an alternating manner that reduces the likelihood of access conflicts between the banks (Fig 2, 116 Intelligent Interleave Scheduler; Col 4, Lines 6-61).

Although Lee does not specifically disclose a plurality of separate linked list data structures for the protocol data units, Beshai teaches a network controller device which stores incoming data as a plurality of separate linked list data structures (the plurality of 506 entries in each 504 Record in Figure 2; Col 6, Lines 2-6) in memory, where the memory is arranged in a plurality of data groupings (Fig 5A, 504 Records 1-N), the data groupings being configured to store respective ones of the plurality of separate linked list data structures, such that each of the plurality of data groups stores a corresponding one of the plurality of separate linked list data structures (Col 6, Lines 2-6; Fig 5A). Beshair's configuration allows dynamic sharing of a memory by the plurality of data groupings and also reduces the size of memory required for storing the received data (Col 6, Lines 25-35). It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that each of Lee's separate groups of protocol data units can be stored as a separate linked list data structure in a corresponding memory

bank, in order to allow dynamic sharing of Lee's memory and reduction of the size of memory required for storing the protocol data units.

It is clear that the method of claim 16 is performed by the processor in claim 1, and it is also clear that the article of manufacture of claim 17 is encompassed in the processor of claim 1, with the method of claim 16 performed by a program code (Intelligent Interleave Scheduler suggests a program, and 102 Network Processor of Fig 2 suggests executing program code) stored in a machine-readable storage medium (the program code must be stored in a storage medium in order for the Network Processor and the Intelligent Interleave Scheduler to read and execute it).

As for claim 2, Lee further teaches that at least a portion of the memory circuitry associated with the processor comprises an external memory connectable to the processor (Fig 2, 114 Memory).

As for claim 3, although Lee does not specifically discloses that at least a portion of the memory circuitry associated with the processor comprises an internal memory of the processor, it is obvious to one ordinarily skilled in the art that a processor generally comprises a cache to increase the speed of execution when accessing data external to the processor, and since Lee's processor includes a Network Processor (Fig 2, 102 Network Processor), it would have been obvious to one ordinarily skilled in the art at the

time of the Applicant's invention that at least a portion of the memory circuitry associated with the processor comprises an internal memory of the processor, in order to improve the speed of execution of the processor.

As for claim 4, Lee further teaches that the memory circuitry comprises a dynamic random access memory (DRAM) (Col 2, Lines 29-31).

As for claim 5, Lee in further view of Beshai already substantially teaches the claim as described above in claim 1, and further teaches that the memory circuitry comprises at least four distinct memory banks (Col 2, Lines 29-32; Fig 1, 114 Multibank Memory, B1-B4), each of the four memory banks storing a corresponding one of four separate linked list data structures (Fig 1 and Fig 3, 114 Multibank Memory, the packets in each bank are already described in claim 1 as separate linked list data structures).

As for claim 6, Lee further teaches the linked list data structures are accessed in an alternating manner by accessing the corresponding memory banks sequentially in accordance with a round-robin selection algorithm (Col 5, Lines 22-31).

As for claim 10, Lee further teaches the protocol data unit comprises a packet (Fig 1, Packet #1 to #4).

As for claim 13, Lee further teaches the processor is configured to provide an interface (Fig 2, 104A-104N Input Queues and 122A-122N Output Queues) for communication of the received protocol data units between a network (Fig 1, 80 Internet) and a switch fabric (Fig 2, 112 FIFO, 120 FIFO, and 116 Intelligent Interleave Scheduler; also see Fig 1).

As for claim 14, Lee further teaches the processor comprises a network processor (Fig 2, 102 Network Processor).

As for claim 15, Lee further teaches the processor is configured as an integrated circuit (Fig 1, 100 System Controller contains a network processor, which must be an integrated circuit).

Allowable Subject Matter

Claims 7-9, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

29 November 2005

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER